I Claim:

1. In a parallel processing system, a method of sending a message across an interconnection network from a first compute node, which has a processor and a memory, to a second compute node, which has a processor and a memory, the method which comprises:

in the first compute node, setting a message header field of the message to a predetermined value and sending the message;

in the second compute node, receiving and processing the message header, and reading a memory location in accordance with contents of a base address register and an index register; and

using Direct Memory Access, storing the message in a memory at a storage address determined in accordance with contents of the memory location.

2. The method according to claim 1, wherein the storage address is aligned on a memory page boundary.

3. The method according to claim 1, which further comprises, with the second compute node, incrementing the index register.

4. The method according to claim 3, which further comprises,

with the second compute node, decrementing a size register indicative of a number of storage addresses stored in a portion of memory.

5. The method according to claim 1, which further comprises, with the second compute node, prior to storing the message, checking the contents of the memory location.

6. The method according to claim 5, which further comprises:

comparing a field of the contents of the memory location with the message header field; and

with a second compute means, storing the message at the storage address only upon obtaining a particular comparison result.

7. The method according to claim 5, which further comprises:

providing the contents of the memory location with a valid bit; and

with the second compute means, storing the message at the storage address only if the valid bit indicates a valid storage address.